REMARKS

The following remarks are provided in response to the Final Office Action mailed April 10, 2006, to the Notice of Appeal filed by the Applicants on June 30, 2006 and to the Interviews of August 14 and 21, 2006 in which the Examiner:

- rejected claims 1-4, 8-9, and 29-34 under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 6,586,808 to Xiang et al. (hereinafter Xiang) in view of United States Patent No. 6,744,101 to Long et al. (hereinafter Long).

Additionally, two new pieces of prior art were raised: Japanese Patent Document No. 05226361 to Matshuhashi (hereinafter Matshuhusi) and US Publication No. 2003/0132466 to Shin et al. (hereinafter Shin).

The applicants respectfully request reconsideration of the above referenced patent application for the following reasons:

Claims 1-4, 8-9, and 29-34 rejection under 35 U.S.C. §103(a)

The Examiner rejected claims 1-4, 8-9, and 29-34 as being unpatentable over Xiang in view of Long. The applicants herein cancel claims 1-4, 8-9, and 29-34 without prejudice.

Interview Summary

The applicants would like to thank the Examiner for taking the time to meet in a phone interview on August 14, 2006 and again on August 21, 2006. During the

interview, two new pieces of prior art were raised: Matshuhashi and Shin. The Applicants address the two new references below and submit Form 1449, filed concurrently herewith.

New Claims 35-50

In claims 35-50, the applicants teach and claim a transistor comprising a dielectric layer above a substrate and a trench in the dielectric layer, wherein the bottom of the trench is directly above the substrate. A gate dielectric layer is in the trench and a first portion of the gate dielectric layer is adjacent to a first sidewall of the trench, a second portion of the gate dielectric layer is adjacent to a second sidewall of the trench and a third portion of the gate dielectric layer is on the bottom of the trench. A gate electrode in the trench and is directly between the first and second portions of the gate dielectric layer. The gate electrode is comprised of a central portion and a pair of outer portions, wherein the central portion is directly adjacent to the pair of outer portions. The bottom surfaces of the central portion and the pair of outer portions of the gate electrode are directly on the third portion of the gate dielectric layer. The workfunction of the pair of outer portions is different than the workfunction of the central portion. Finally, a pair of source/drain regions is in the substrate on opposite sides of the pair of outer portions of the gate electrode. That is, the applicants teach and claim a transistor having **a gate electrode comprising a central portion and a pair of outer portions, wherein the central portion is directly adjacent to the pair of outer portions, and wherein all portions of the gate electrode are directly between two portions of a gate dielectric**

layer and directly above a third portion of the gate dielectric layer (gate dielectric layer with three portions: *see* item "210", Fig. 2 and item "318", Figs. 3F-3K).

In claims 35-42, the transistor is an NMOS transistor, the workfunction of said pair of outer portions is lower than the workfunction of said central portion, and the pair of source/drain regions is a pair of n type source/drain regions. In claims 43-50, the transistor is a PMOS transistor, the workfunction of said pair of outer portions is higher than the workfunction of said central portion, and the pair of source/drain regions is a pair of p type source/drain regions.

Xiang, Long, Matshuhashi and Shin all disclose transistors having a gate electrode comprising a central portion and a pair of outer portions, wherein the bottom surfaces of all portions are above a portion of a gate dielectric layer. However, **none of these references disclose a transistor wherein all portions of the gate electrode are <u>in between</u> two additional portions of the same gate dielectric layer**, as taught by the applicants. The applicants teach fabricating a transistor by a total replacement gate dielectric layer process scheme, whereas the transistors in Xiang, Long, Matshuhashi and Shin are fabricated by subtractive, selective growth, planar layer (i.e. a gate dielectric layer that is deposited or grown on a planar surface as opposed to in a trench) or partial replacement gate dielectric layer process schemes. For example, the transistors in Xiang are fabricated by a subtractive gate dielectric process (*see* Figs. 3A-B) or a partial replacement gate dielectric layer process (*see* Figs. 6C-6D). The transistors in Long are fabricated by a subtractive gate dielectric process (*see* Figs. 4(4b)-4(5)) or a selective growth process (*see* Figs. 5(2)-5(4) and 6(2)-6(3)). The transistors in Matshuhashi are

fabricated by a planar layer gate dielectric layer process (*see* Figs. 4A-C). Finally, the transistors in Shin are fabricated by a planar layer gate dielectric layer process (*see* Figs. 4-11). Thus none of Xiang, Long, Matshuhashi nor Shin would have been motivated to fabricate a transistor having **all portions of a gate electrode between two portions of a gate dielectric layer**, as taught by the applicants.

Therefore, none of Xiang, Long, Matshuhashi nor Shin alone, or in combination, disclose a transistor having a gate electrode comprising a central portion and a pair of outer portions, wherein the central portion is directly adjacent to the pair of outer portions, and wherein all portions of the gate electrode are directly between two portions of a gate dielectric layer and directly above a third portion of the gate dielectric layer, as taught by the applicants.

CONCLUSION

The applicants submit that they have overcome the Examiner's claim rejections and that they have the right to claim the invention as set forth in the listed claims. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,

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8/25/06

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